Accelerated Nios II/e Tiny Embedded System ecosystem (fits in the smallest Cyclone 10 FPGA device)

Implemented on Intel Cyclone 10 FPGA evaluation board but can be readily adapted for use with any Intel MAX10 and Cyclone 10 LP FPGA devices.

A simple reference design for accelerating the Nios II/e processor using S/Labs' System Cache. It also features Arduino style key components and pin headers, such as PIO, SPI, and I2C interfaces.

In addition, it supports an 16 Mbyte HyperRAM and a 8 Mbyte EPCQ memory with very low pin count.

The total embedded system fits in the

Embedded system components

- 100 Mhz design
- 12 pins for HyperRam
- 2 shared pins for I2C slaves

https://cloud.altera.com/devstore/platform/17.0.0/Standard/accelerated-nios-iiie-embedded-system/
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